I claim:

1. An integrated circuit comprising;

a test data input terminal and a test data output terminal;

a boundary scan path including a mixture of serially connected dedicated and shared boundary scan cells, said boundary scan path having an input and an output;

a first connection formed between said test data input terminal and said boundary scan path input, and;

a second connection formed between said test data output terminal and said boundary scan path output.

2. An integrated circuit comprising;

a boundary scan path including one or more groups of serially connected dedicated boundary scan cells and one or more groups of serially connected shared boundary scan cells, said boundary scan path having an input and an output; and

multiplexer circuitry associated with said boundary scan path for selectively bypassing said one or more shared boundary scan cell groups such that only the one or more dedicated boundary scan cell groups exist between said input and output.

3. The integrated circuit of claim 2 further comprising;

a test data input terminal and a test data output terminal;

a first connection formed between said test data input terminal and said boundary scan path input, and;

a second connection formed between said test data output terminal and said boundary scan path output.

4. The integrated circuit of claim 2 further comprising;

at least one resynchronization memory located in the serial path between at least two of said dedicated boundary scan cell groups.

5. An integrated circuit comprising;

a first boundary scan path portion having an input and an output and one or more dedicated scan cells coupled therebetween;

a second boundary scan path portion having an input and an output and one or more shared scan cells coupled therebetween;

a multiplexer having first and second inputs;

a first connection formed between the output of said first boundary scan path portion and said first multiplexer input;

a second connection formed between the output of said second boundary scan path portion and said second multiplexer input; and,

a third connection formed between the output of said first boundary scan path portion and said input to said second boundary scan path portion.

6. The integrated circuit of claim 5 further comprising;

a least one resynchronization memory located in the first connection formed between the output of said first boundary scan path portion and said first multiplexer input.

7. An integrated circuit comprising;

a boundary scan path having at least one resynchronization memory located in the serial path between two boundary scan cells.

8. A process of entering into a boundary scan test mode comprising the steps of;

performing a first serial communication to load data into only a subset of the scan cells within the boundary scan path,

entering the boundary scan test mode, and;

performing a second serial communication to load data into all the scan cells within the boundary scan path.

9. An intellectual property core circuit within an integrated circuit, said intellectual property core circuit comprising;

a boundary scan path having an input and an output, said boundary scan path containing a mixture of serially connected shared and dedicated scan cells; and

multiplexer circuitry for selectively partitioning the boundary scan path to include only the dedicated scan cells between said input and output.

10. An integrated circuit comprising

a test data input terminal and a test data output terminal;

a plurality of intellectual property core circuits each including a boundary scan path containing and input lead and an output lead and a mixture of dedicated and shared scan cells located serially between said input and output leads;

connections formed between the input and output leads of the boundary scan paths such that the output of a leading boundary scan path connects to an input of a trailing boundary scan path to form a serial arrangement of boundary scan paths;

an input connection formed between the test data input terminal and the input lead of the first boundary scan path of said serial arrangement of boundary scan paths; and

an output connection formed between the test data output terminal and the output lead of the last boundary scan path of said serial arrangement of boundary scan paths.

11. A boundary scan system comprising:

A. a test data input;

B. a test data output;

C. at least one control scan cell having a memory capable of scanning a test signal while carrying a functional signal;

D. at least one data scan cell having a memory that is used for both test and functional signals;

E. a boundary scan path between the test data input and the test data output, the path having two configurations, the first configuration including the at least one control scan cell and excluding the at least one data scan cell, and the second configuration including both the at least one control scan cell and the at least one data scan cell; and

F. a multiplexer in the path selecting between the first and second configurations.